Interfacing The EISCAT KST Antenna to The VMEbus

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Purpose is to interface the existing UHF Antenna Control to the VMEbus. Old specifications and data formats of existing ACU and Polarizer will be shown.

The General purpose VME digital I/O board MPV924 by Pentland[4] is chosen. Specifications and some hardware configuration will be given. Also some control bit distribution will be discussed.

1- KST ANTENNA CONTROL UNIT (ACU)

Communication with the ACU is positive true logic in parallel Form using differential line drivers (DS8831)[1] and differential line receivers (DS8820)[2]. Single ended operation is used, making connections only to the positive or negative logic input and output.

Logic Level 1	+3.5V Min.
Logic Level 0	+1. 5V Max
Drive Sink and Source Currents	40 mA Max
Receiver Input Current	1 mA Max.

DATA FORMAT

The total command from the MVP924 to the antenna control unit (ACU) shall consist of 24 bits allocated as:

Transmit Word to the ACU:

BIT #	DESCRIPTION	MPV SIGNAL	ACU PIN # J1
1	Data, LSB	TD0	1
2	Data	TD1	3
3	Data	TD2	5
4	Data	TD3	7
5	Data	TD4	9
6	Data	TD5	11
7	Data	TD6	13
8	Data	TD7	15
9	Data	TD8	17
10	Data	TD9	19
11	Data	TD10	21
12	Data	TD11	23
13	Data	TD12	25
14	Data	TD13	27
15	Data	TD14	29
16	Data	TD15	31
17	Data, MSB	TD16	33
21	Address, LSB	TA0	41
20	Address	TA1	39
19	Address	TA2	37
18	Address. MSB	TA3	35

22	Read/Write	R/W		43
23	Parity	PAR T		45
24	Strobe	STROBE	0 → 1	47

The total feedback from the ACU to the MVP924 shall consist of 2 interrupt and 23 bits allocated as:

Receive Word from the ACU: (Data must be inverted due to compatibility)

BIT #	DESCRIPTION	MPV SIGNAL	ACU PIN # J2
1	Data, LSB	RD0	2
2	Data	RD1	4
3	Data	RD2	6
4	Data	RD3	8
5	Data	RD4	10
6	Data	RD5	12
7	Data	RD6	14
8	Data	RD7	16
9	Data	RD8	18
10	Data	RD9	20
11	Data	RD10	22
12	Data	RD11	24
13	Data	RD12	26
14	Data	RD13	28
15	Data	RD14	30
16	Data	RD15	32
17	Data, MSB	RD16	34
21	Address Ident, LSB	RA0	42
20	Address Ident	RA1	40
19	Address Ident	RA2	38
18	Address Ident, MSB	RA3	36
22	Set Complete	S/C	44
23	Parity	PAR R	46
24	Data Interrupt (Set Complete)	D/I	48
25	Command Interrupt (Disable)	C/I	50

The Transmit Word, Control Word, Receive Word and Interrupts travel via separate wires (49 total paths) between the ACU and the MVP924. Each I/0 is configured for a bus type organization so that additional axes or sub-modes may be added at a later date.

ADDRESSING

A 4-bit address code is used giving a maximum capability of 15 addresses. Zero is not used since an open cable will result in a zero address on the line receiver outputs.

	MSB			LSB	
BIT#	18	19	20	21	
MPV	TA3	TA2	TA1	TA0	
	1	1	1	1	Azimuth
	1	1	1	0	Elevation
	1	1	0	1	Horn Alarm
	1	1	0	0	Set Standby
	1	0	1	1	Set Computer

ADDRESS IDENT (RA0-RA3)

The address of the axis or sub-mode responding to a READ command is presented on the Address Ident Line to identify the source of the DATA on the DATA bus.

READ/WRITE

This bit, when set to "1", will cause the WRITE function to occur. When the bit is set to "0", the READ function occurs. WRITE function the ACU will accept a position command when:

a) Address is decoded
b) READ/WRITE Bit is “1”
c) Parity is correct
d) Strobe goes-from “0” to “1”

When the strobe is high, the output of the ACU command register is connected to the Receive Word line drivers. The accepted command is available for comparison to sent command within 1 usec of the strobe reading edge and remains available while the strobe is high.

READ function - the ACU will enable the Receive Word line drivers when:

a) Address is decoded
b) READ/WRITE Bit is “0”
c) Parity is correct.
d) Strobe is "1"

The present position data will be valid within 2 usec of the strobe leading edge and remains available while the strobe is high.

PARITY

Odd parity is used. The input parity includes bit 1 through 22 of the Transmit and Control Words for the WRITE function. Input parity is based on bits 1 through 22 for the READ function. The output parity includes bits 1 through 22 of the Receive Word. Although bits 1 - 17 are "don't care" for read command, parity is still computed on them.

STROBE

A minimum of 1 usec settling time shall be allotted between application of data/ address/ write/read and the strobe going from '.0" to "1". The strobe shall remain high a minimum of 2 usecs.

INTERRUPTS

Two interrupts are provided, (a) set complete, (b) axis disabled. The interrupts are set high when the condition occurs and are reset low by the strobe or termination of the condition.

a) Set Complete - The set complete interrupt is set high when the position command has been satisfied. When reset by the strobe, it will not be set high until a new command has been entered and satisfied. A status bit is provided.

b) Axis Disabled - The axis disable interrupt is set high when a fault occurs. When reset by the strobe, it will not be set high until the condition clears and re-occurs. Status is indicated by responding with an address of zero when poled. An enabled unit will respond with its correct address. The computer interface card (VME MPV 924) should be configured to inter-pret an off tri-state line driver as a zero.

For multiple axis systems, the interrupts will be “wired or” and it will be necessary to pole to determine who interrupted.

SET COMPLETE

The Set Complete Bit is set to "1" when the present position of the axis is in agreement with the last position command.

ACU DISABLED

Disabled Bit is set to "1" whenever the ACU is incapable of responding to computer commands. It can be caused by any of the following:

1) Source Select switch not in "computer"
2) Limit switch activated
3) Emergency switches activated
4) Internal fault, such as loss of synchro voltage
5) Drive fault

COMPUTER VELOCITY CONTROL

The axis velocity in track mode is controlled by the following expression:

Vel = K (e) 1/2 $\leq$ 100/minutes

where e = position error. The value of K will be determined by final loop compensation. Therefore, by maintaining a small position error on a sampling basis, velocity control can be achieved. The smoothness depends upon sampling rate and axis inertia.

PRESENT POSITION

Axis present position will be loaded into the command registers upon power-on or switching into COMPUTER control mode. This will prevent any mechanical movement until a valid command has been received from the computer.

WARNING HORN INTERFACE

Warning Horn Address

BIT#	18	19	20	21
MPV	TA3	TA2	TA1	TA0
	1	1	0	1

Horn will sound for 10 seconds when

a) Warning horn address is on address-lines
b) Read/Write Bit Is 1
c) Parity is correct
d) Strobe goes from "0" to "1"

2- KST ANTENNA POLARIZER CONTROL

The polarizer control is identical for all three UHF-antennas. Polaritzation can be controlled with an external parallel input at TTL –logic levels.

Communication with the MVP924 is positive true logic in parallel Form using differential line drivers (DS8830)[1] and differential line receiver (DS8820)[2]. Single ended operation is used making connections only to the positive logic inputs.

ELECTRICAL CHARACTERISTICS

Logic Level 1	+3.5V Min.
Logic Level 0	+1. 5V Max
Drive Sink and Source Currents	40 mA Max
Receiver Input Current	1 mA Max.

DATA FORMAT

The range of the amplitude ratio is limited by the 8 bit representation with 7 bit as magnitude and 1 bit as sign from –127 to +127 quarter dB steps at J3. RUN/STOP input is a possibility to disable the drive to the amplitude control phase shifter. The ready output gives an indicator that the phase sifter 1 of the polarizer has reached the wanted position. Wiring of connector J3:

Transmit word for Amplitude:

BIT #	DESCRIPTION	MPV SIGNAL	PIN NUMBER J3
1	Amplitude data 0 LSB	TDA0	B
2	Amplitude data 1	TDA1	D
3	Amplitude data 2	TDA2	F
4	Amplitude data 3	TDA3	H
5	Amplitude data 4	TDA4	K
6	Amplitude data 5	TDA5	M
7	Amplitude data 6 MSB	TDA6	P
	GND		p
8	Amplitude sign	TDA7	S
	GND		r
1	RUN/STOP AMP	ARUN	W
	GND		s
2	READY	ARDY	X

The remote input for the phase is a 9 bit number at J2. Phase values from 0 to 360 degrees are expected. The RUN/STOP input disables the drive of phase shifter 2 and the ready output indicates that the phase shifter 2 has reached the wanted position. The wiring of connector J2:

Transmit word for Phase:

BIT #	DESCRIPTION	MPV SIGNAL	PIN NUMBER J2
1	Phase data 0 LSB	TDP0	B
2	Phase data 1	TDP1	D
3	Phase data 2	TDP2	F
4	Phase data 3	TDP3	H
5	Phase data 4	TDP4	K
6	Phase data 5	TDP5	M
7	Phase data 6	TDP6	P
8	Phase data 7	TDP7	S
	GND		p
9	Phase data 8 MSB	TDP8	U
	GND		r
1	RUN/STOP PHA	PRUN	W
	GND		s
2	READY	PRDY	X

3- VME DIGITAL I/O BOARD MPV 924

Key Features:

- 96 digital inputs / outputs
- Channels can be software configured in groups of eight I/O:s
- 16 channels with software programmable "change of state" response (COS)
- 7 levels of VMEbus interrupt, selectable through software
- Software relocation of functional memory map
- Software reset register
- Output connectors six 34-way IDC connectors P3…P8
- Software selectable address modifier response
- System configuration map (size 128 words)
- Functional memory map (size 128 words)

ELECTRICAL CHARACTERISTICS

Digital Inputs (receiver type is 74LS374 and for COS-inputs 74LS244)

Logic level	"1"	2.0 V
Logic level	"0"	0.8 V
Input current	"1"	60 uA
Input current	"0"	-0.62 mA

Digital Outputs (driver type is 74LS374)

Logic level	"1"	2.4 V
Logic level	"0"	0.5 V
Output current	"1"	-2.6 mA
Output current	"0"	24 mA

DIGITAL I/O REGISTERS

I/O-register is 96 bits wide arranged as 6 x 16 bit registers starting at offset address +C0(H). Bits are allocated as shown:

Hex	byte 0								byte 1								
+C0	CH15 RD16	R PAR			RA3	RA2	RA1	CH8 RA0	CH7			PRDY	ARDY	C/I	D/I	CH0 B/C	IN /COS
+C2	CH31 RD15	RD14	RD13	RD12	RD11	RD10	RD9	CH24 RD8	CH23 RD7	RD6	RD5	RD4	RD3	RD2	RD1	CH16 RD0	IN
+C4	CH47 TD15	TD14	TD13	TD12	TD11	TD10	TD9	CH40 TD8	CH39 TD7	TD6	TD5	TD4	TD3	TD2	TD1	CH32 TD0	OUT /INV
+C6	CH63 TD16	T PAR			TA3	TA2	TA1	CH56 TA0	CH55						STRO BE	CH48 R/W	OUT /INV
+C8	CH79							CH72 ARUN	CH71 TDA7	TDA6	TDA5	TDA4	TDA3	TDA2	TDA1	CH64 TDA0	OUT
+CA	CH95						PRUN	CH88 TDP8	CH87 TDP7	TDP6	TDP5	TDP4	TDP3	TDP2	TDP1	CH80 TDP0	OUT

DIGITAL I/O CONNECTIONS (CH00-CH96)

Each digital I/O channel is accessed via one of the six 34-way latching IDC connectors. The pin-outs of these connectors P3, P4, P5, P6, P7, and P8 are in next lines.

P3

CH15	34	33	GND
CH14	32	31	GND
CH13	30	29	GND
CH12	28	27	GND
CH11	26	25	GND
CH10	24	23	GND
CH09	22	21	GND
CH08	20	19	GND
CH07	18	17	GND
CH06	16	15	GND
CH05	14	13	GND
CH04	12	11	GND
CH03	10	09	GND
CH02	08	07	GND
CH01	06	05	GND
CH00	04	03	GND
+5V	02	01	GND

P4

CH31	34	33	GND
CH30	32	31	GND
CH29	30	29	GND
CH28	28	27	GND
CH27	26	25	GND
CH26	24	23	GND
CH25	22	21	GND
CH24	20	19	GND
CH23	18	17	GND
CH22	16	15	GND
CH21	14	13	GND
CH20	12	11	GND
CH19	10	09	GND
CH18	08	07	GND
CH17	06	05	GND
CH16	04	03	GND
+5V	02	01	GND

P5

CH47	34	33	GND
CH46	32	31	GND
CH45	30	29	GND
CH44	28	27	GND
CH43	26	25	GND
CH42	24	23	GND
CH41	22	21	GND
CH40	20	19	GND
CH39	18	17	GND
CH38	16	15	GND
CH37	14	13	GND
CH36	12	11	GND
CH35	10	09	GND
CH34	08	07	GND
CH33	06	05	GND
CH32	04	03	GND
+5V	02	01	GND

P6

CH63	34	33	GND
CH62	32	31	GND
CH61	30	29	GND
CH60	28	27	GND
CH59	26	25	GND
CH58	24	23	GND
CH57	22	21	GND
CH56	20	19	GND
CH55	18	17	GND
CH54	16	15	GND
CH53	14	13	GND
CH52	12	11	GND
CH51	10	09	GND
CH50	08	07	GND
CH49	06	05	GND
CH48	04	03	GND
+5V	02	01	GND

P7

CH79	34	33	GND
CH78	32	31	GND
CH77	30	29	GND
CH76	28	27	GND
CH75	26	25	GND
CH74	24	23	GND
CH73	22	21	GND
CH72	20	19	GND
CH71	18	17	GND
CH70	16	15	GND
CH69	14	13	GND
CH68	12	11	GND
CH67	10	09	GND
CH66	08	07	GND
CH65	06	05	GND
CH64	04	03	GND
+5V	02	01	GND

P8

CH95	34	33	GND
CH94	32	31	GND
CH93	30	29	GND
CH92	28	27	GND
CH91	26	25	GND
CH90	24	23	GND
CH89	22	21	GND
CH88	20	19	GND
CH87	18	17	GND
CH86	16	15	GND
CH85	14	13	GND
CH84	12	11	GND
CH83	10	09	GND
CH82	08	07	GND
CH81	06	05	GND
CH80	04	03	GND
+5V	02	01	GND

Termination resistors are located on EISCAT customise board, if needed

Upon power-up, after a SYSRESET or after a SOFTRESET – (generated trough the system memory map), all software programmable registers are reset to 00(H) and all digital I/O channels are configured as inputs.

THE BASE ADDRESS

The system configuration memory map of MVP924 occupies 128 words of memory at any one of 256 offset locations within the VME short I/O space. The location of the VME short I/O space is made for Spark 2CE CPU of FORCE COMPUTER[7].

The base address of the system configuration memory map is determined from the VME short address, plus an offset which is selected using jumper J2.

	a	on		
	b	on	**Configured:**	12.01.1998
	c	on		
J2	d	on	**Base address:**	FFFF 1000
	e	out		
	f	on		
	g	on		
	h	on		

SUPERVISORY OR NON PRIVILEGED ACCESS

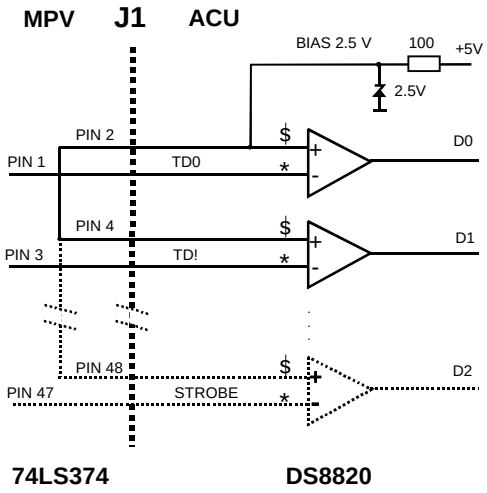
Jumper J1 is used to select the system configuration map address modifier response and can be used to restrict accesses to this area of memory.

J1	a	on	**Configured:**	12.01.1998

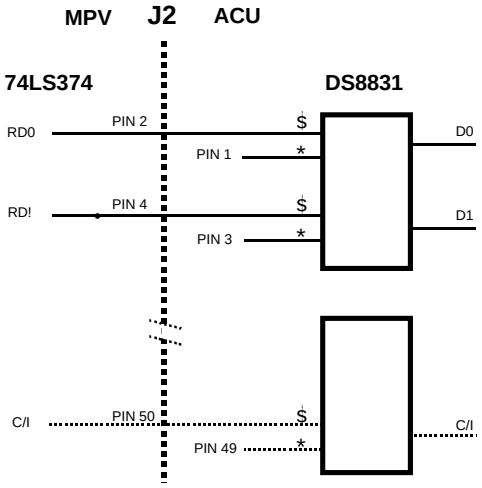
When jumper J1 is removed the board will respond to CPU´s operating in supervisory or non-privileged mode. When inserted, only CPU´s operating in supervisory mode may access the system configuration registers.

Line receivers in the ACU

TRANSMIT TO THE ACU

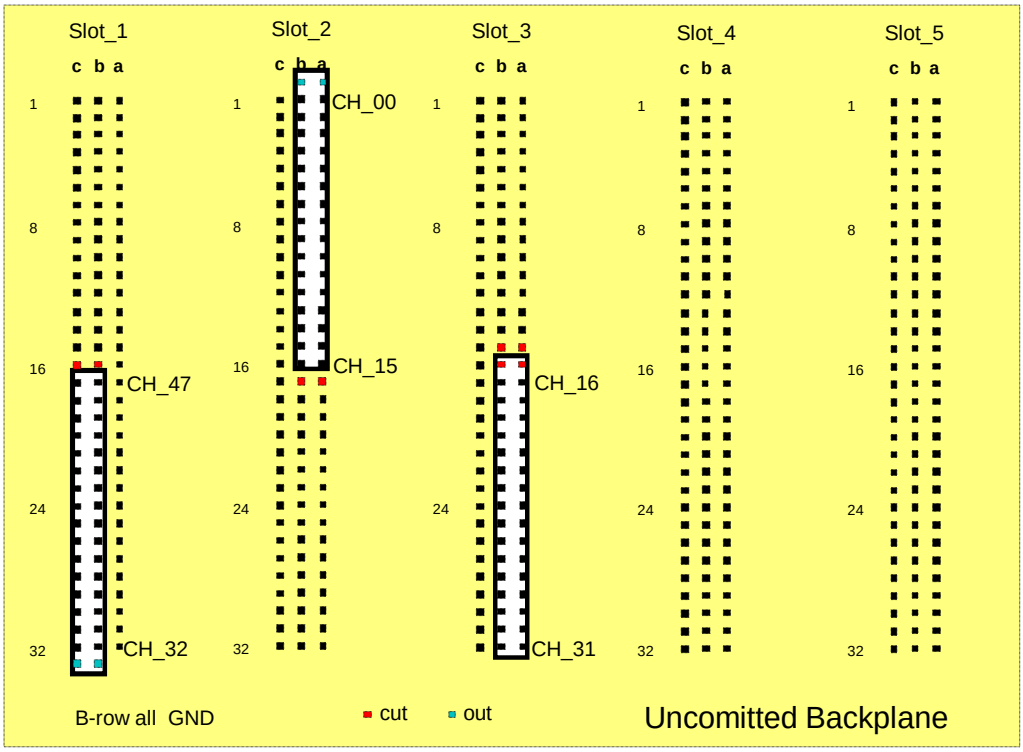


Line drivers in the ACU

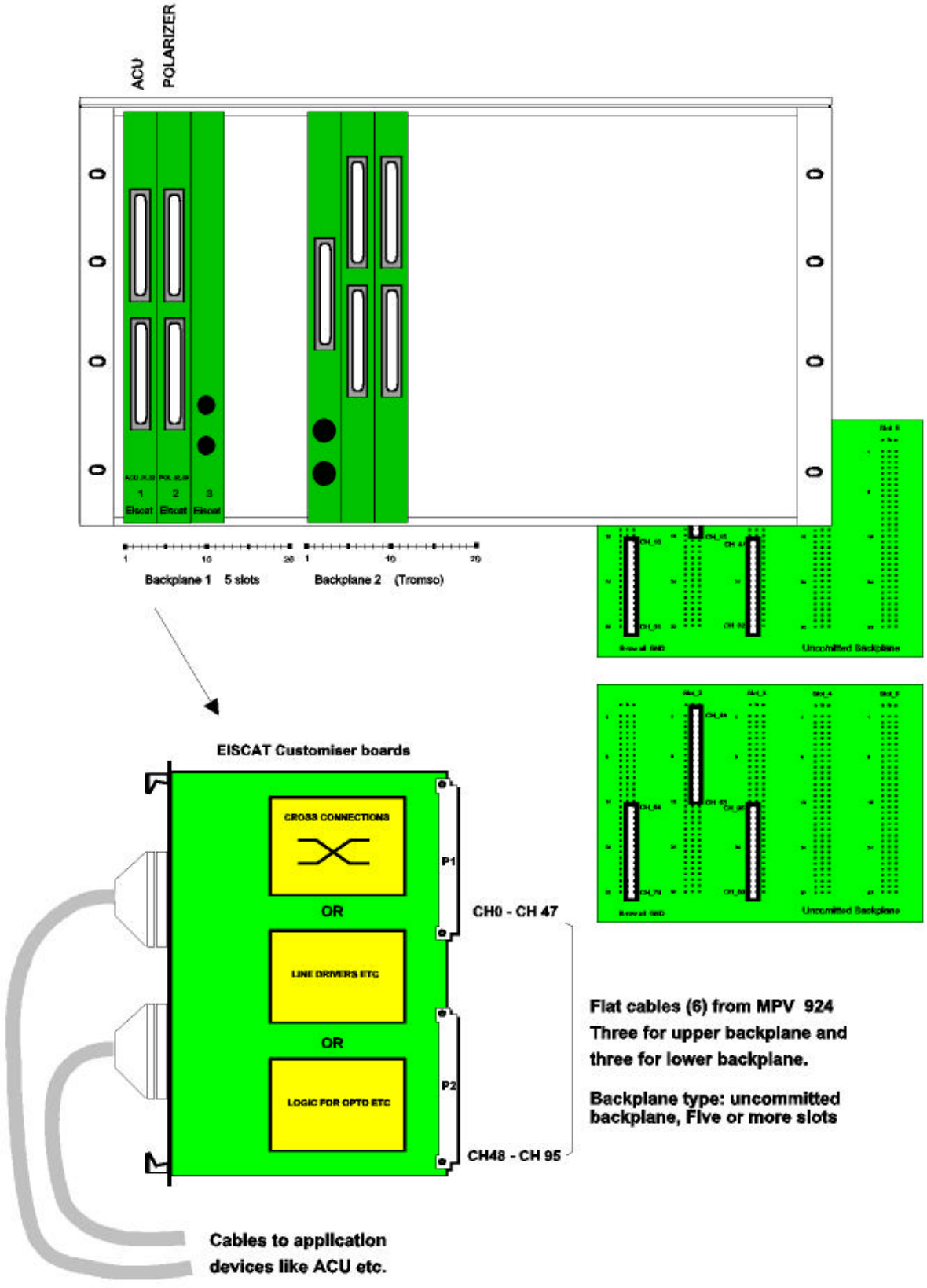


4- CABLES AND CONNECTIONS, CUSTOMISER BOARD

In MPV924 digital I/O signals (CH00-CH95) are applied to the six 34-way IDC connectors P3, P4, P5, P6, P7, and P8. Connectors are wired by Twisted pair flatcable down to the uncommitted backplane where all signals are available. One backplane can easily hold 64 signals and one row is reserved for grounding, so we need both connectors 48 signal on both..



New Cables are made for full compatibility and mating with the ACU- and POLARITZER-cables.


ACU
POLARIZER
1 Elcat
2 Elcat
3 Elcat
Backplane 1 5 slots
Backplane 2 (Tromso)
Uncomitted Backplane
Uncomitted Backplane
EISCAT Customiser boards
CROSS CONNECTIONS
OR
LINE DRIVERS ETC
OR
LOGIC FOR OPTO ETC
P1
P2
CH0 - CH 47
CH48 - CH 95
Flat cables (6) from MPV 924
Three for upper backplane and
three for lower backplane.
Backplane type: uncommitted
backplane, Five or more slots
Cables to application
devices like ACU etc.

EISCAT KST Radar
Receiver Digital I/O

PIN-Assignments for
E1 and E2-connector

Date: 14.03.2000/TL

Customiser Boards **KST-DIGITAL I/O**

Position: Digital I/O Backplane 1 and 2

E 1/II			
PIN	ROW a	ROW b	ROW c
No:	Signal	Signal	Signal
1	CH00	GND	(+)5V/10A
2	CH01	GND	(+)5V/10A
3	CH02	GND	(+)5V/10A
4	CH03	GND	
5	CH04	GND	
6	CH05	GND	(-)5V/1A
7	CH06	GND	(-)5V/1A
8	CH07	GND	
9	CH08	GND	(+)15V/4A
10	CH09	GND	(+)15V/4A
11	CH10	GND	
12	CH11	GND	(-)15V/1A
13	CH12	GND	(-)15V/1A
14	CH13	GND	
15	CH14	GND	
16	CH15	GND	
17	CH16	GND	CH47
18	CH17	GND	CH46
19	CH18	GND	CH45
20	CH19	GND	CH44
21	CH20	GND	CH43
22	CH21	GND	CH42
23	CH22	GND	CH41
24	CH23	GND	CH40
25	CH24	GND	CH39
26	CH25	GND	CH38
27	CH26	GND	CH37
28	CH27	GND	CH36
29	CH28	GND	CH35
30	CH39	GND	CH34
31	CH30	GND	CH33
32	CH31	GND	CH32

E2/II			
PIN	ROW a	ROW b	ROW c
No:	Signal	Signal	Signal
1	CH48	GND	
2	CH49	GND	
3	CH50	GND	
4	CH51	GND	
5	CH52	GND	
6	CH53	GND	
7	CH54	GND	
8	CH55	GND	
9	CH56	GND	
10	CH57	GND	
11	CH58	GND	
12	CH59	GND	
13	CH60	GND	
14	CH61	GND	
15	CH62	GND	
16	CH63	GND	
17	CH64	GND	CH95
18	CH65	GND	CH94
19	CH66	GND	CH93
20	CH67	GND	CH92
21	CH68	GND	CH91
22	CH69	GND	CH90
23	CH70	GND	CH89
24	CH71	GND	CH88
25	CH72	GND	CH87
26	CH73	GND	CH86
27	CH74	GND	CH85
28	CH75	GND	CH84
29	CH76	GND	CH83
30	CH77	GND	CH82
31	CH78	GND	CH81
32	CH79	GND	CH80

emarks:

( ) Not used

Cables between Connection I/O Board and ACU, Polarizer

Cable between C-I/O board and ACU is ONE TO ONE, pin to pin. Connector on ACU is 50-pin D-connector, C-I/O connector is 50-pin IDC connector (J1 and J2).

Connector on Polarizer is 28-2PR and on C-I/O board is 34-pin IDC connector. Cable Between C-I/O board and Polarizer:

Polarizer J2 and J3	Connection I/O Board J2 and J3
A	1
B	2
C	3
D	4
E	5
F	6
G	7
H	8
J	9
K	10
L	11
M	12
N	13
P	14
R	15
S	16
T	17
U	18
V	19
W	20
X	21
Z	22
a	23
b	24
-	25
-	26
-	27
-	28
-	29
-	30
-	31
p	32
r	33
s	34

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