The descriptions of the bits of RC memory row (32+6 bits) of the ESR-RX radar controller for DSP1 grate:

Bit N:o	Signal	Direction	Description	Destination
61	Spare	-	-	-
60	IFSEL	Output	IF box select bit	IF switch box
59	SPARE	-	-	-
58	AD_sel1	Output	Selects AD1 or AD2 data	Data drivers 1-3
57	AD_sel2	Output	Selects AD1 or AD2 data	Data drivers 4-6
56	SPARE	-	-	-
31	Rx-sync			
30	NCO-reset	O, neg. pulse	Zeroes NCO phase accumulator	Channel boards
29	NCO-load	O, pos. pulse	Activates frequency loading logic	Channel boards
28	NCO-select -9	Output	Numerical Control Oscillator freg. select bit 9	Channel boards
27	NCO-select -8	Output	Numerical Control Oscillator freg. select bit 8	Channel boards
26	NCO-select -7	Output	Numerical Control Oscillator freg. select bit 7	Channel boards
25	NCO-select -6	Output	Numerical Control Oscillator freg. select bit 6	Channel boards
24	NCO-select -5	Output	Numerical Control Oscillator freg. select bit 5	Channel boards
23	NCO-select -4	Output	Numerical Control Oscillator freg. select bit 4	Channel boards
22	NCO-select -3	Output	Numerical Control Oscillator freg. select bit 3	Channel boards
21	NCO-select -2	Output	Numerical Control Oscillator freg. select bit 2	Channel boards
20	NCO-select -1	Output	Numerical Control Oscillator freg. select bit 1	Channel boards
19	NCO-select -0	Output	Numerical Control Oscillator freg. select bit 0	Channel boards
18	Bufflip II	O, neg. pulse	Changes the role of buffer memory sides	Channel boards 5-8
17	Bufflip I	O, neg. pulse	Changes the role of buffer memory sides	Channel boards 1-4
16	STFIR	O, neg. pulse	Start pulse for FIR filters	Channel boards
15	CHON 6	O, neg. active	Dis/enables data writing into the BM 6	Channel board 6
14	CHON 5	O, neg. active	Dis/enables data writing into the BM 5	Channel board 5
13	CHON 4	O, neg. active	Dis/enables data writing into the BM 4	Channel board 4
12	CHON 3	O, neg. active	Dis/enables data writing into the BM 3	Channel board 3
11	CHON 2	O, neg. active	Dis/enables data writing into the BM 2	Channel board 2
10	CHON 1	O, neg. active	Dis/enables data writing into the BM 1	Channel board 1
9	Spare	-	-	-
8	INT	O, pos. pulse	Interrupt to DSP	CH adapter board
7	CHON8	O, neg.active	Dis/enables data writing into the BM 8	Channel board 8
6	CHON7	O, neg active	Dis/enables data writing into the BM 7	Channel board 7
5	AD_STR	O , pos.pulse	Strobe for AD_sel register	All Data drivers
4	Spare	-	-	-
3	S3	Output	Status bit 3 to DSP interface boards	DSP int. board 1-3
2	S2	Output	Status bit 2 to DSP interface boards	DSP int. board 1-3
1	S1	Output	Status bit 1 to DSP interface boards	DSP int. board 1-3
0	S0	Output	Status bit 0 to DSP interface boards	DSP int. board 1-3
	PatchClk *)	O, pos. pulse	Strobes the RC register DSP int. board 1-2	

1) Pins are defined in the RC pin assignment document (rows P2 a1-a32 and P2 c1- c32).
*) Separate signal from the RC.

O =output, BM = Buffer Memory 31.3.2004

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