The descriptions of the bits of the RC memory row (32+6 bits) of the ESR-RX radar controller for DSP2 grate:

Bit N:o	Signal	Direction	Description	Destination
	LPRPint	Not programmable		
61	Spare			
60	Spare			
59	Spare			
58	Spare			
57	Spare	-	-	-
56	Spare	-	-	-
31	Rx-sync			
30	NCO-reset	O, neg. pulse	Zeroes NCO phase accumulator	Channel boards
29	NCO-load	O, pos. pulse	Activates frequency loading logic	Channel boards
28	NCO-select -9	Output	Numerical Control Oscillator freg. select bit 9	Channel boards
27	NCO-select -8	Output	Numerical Control Oscillator freg. select bit 8	Channel boards
26	NCO-select -7	Output	Numerical Control Oscillator freg. select bit 7	Channel boards
25	NCO-select -6	Output	Numerical Control Oscillator freg. select bit 6	Channel boards
24	NCO-select -5	Output	Numerical Control Oscillator freg. select bit 5	Channel boards
23	NCO-select -4	Output	Numerical Control Oscillator freg. select bit 4	Channel boards
22	NCO-select -3	Output	Numerical Control Oscillator freg. select bit 3	Channel boards
21	NCO-select -2	Output	Numerical Control Oscillator freg. select bit 2	Channel boards
20	NCO-select -1	Output	Numerical Control Oscillator freg. select bit 1	Channel boards
19	NCO-select -0	Output	Numerical Control Oscillator freg. select bit 0	Channel boards
18	ADSEL_1	O, level pos/neg	Selects ADC 1 or ADC 2 for channels 4-6	Channel boards 4-6
17	Bufflip	O, neg. pulse	Changes the role of buffer memory sides	Channel boards
16	STFIR	O, neg. pulse	Start pulse for FIR filters	Channel boards
15	CHON 6	O, neg. active	Dis/enables data writing into the BM 6	Channel board 6
14	CHON 5	O, neg. active	Dis/enables data writing into the BM 5	Channel board 5
13	CHON 4	O, neg. active	Dis/enables data writing into the BM 4	Channel board 4
12	CHON 3	O, neg. active	Dis/enables data writing into the BM 3	Channel board 3
11	CHON 2	O, neg. active	Dis/enables data writing into the BM 2	Channel board 2
10	CHON 1	O, neg. active	Dis/enables data writing into the BM 1	Channel board 1
9	ADSEL_0	O, level pos/neg	Selects ADC 1 or ADC 2 for channels 1-3	Channel boards 1-3
8	INT	O, pos. pulse	Interrupt to DSP	CH-adapter board
7	AD_strobe	O, neg. pulse	Strobe of ADC select register	Channel boards
6	Spare(CH7)	O, neg active	Can be used to CHON 7 if needed	
5	GATE_A	O, pos. pulse	ADC samplegate via Frequency Patch	Pentek 6420
4	GATE_B	O, pos. pulse	ADC samplegate via Frequency Patch	Pentek 6420
3	S3	Output	Status bit 3 to DSP interface boards	CH-adapter board
2	S2	Output	Status bit 2 to DSP interface boards	CH-adapter board
1	S1	Output	Status bit 1 to DSP interface boards	CH-adapter board
0	S0	Output	Status bit 0 to DSP interface boards	CH-adapter board
	PatchClk *)	O, pos. pulse	Strobes the RC register on CH-adapter board	

1) Pins are defined in the RC pin assignment document (rows P2 a1-a32 and P2 c1- c32).
*) Separate signal from the RC.

O =output, BM = Buffer Memory 31.3.2004

G:\cad\hardwork\kstradar\newrc\rcbits_kst.doc O:\httpd\