RW0/1 truth table

18.1.2007

Function	CH95 ISAFUD	CH94 IESYNC	CH93 Reset	CH92 Clock F	CH91 Clock A	CH90 Clock D	CH89 R/WE1	CH88 R/WE0	CH87 RB_enable2	CH86 RB_enable1	CH85 ASF_counter	CH84 ASF_RAM2	CH83 ASF_RAM1	CH82 Boarsel 2	CH81 Boarsel 1	CH80 Boarsel 0
Din Driver enabled							0	0	serial write to DDS							
Generate we-pulse							0	1	RAM, registers loading							
Generate we-pulse							1	0	RAM, registers loading							
Din Driver disabled							1	1	State, when RC is running							

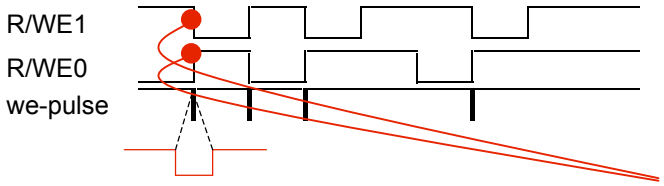
RB1/2 truth table

Function	CH95 ISAFUD	CH94 IESYNC	CH93 Reset	CH92 Clock F	CH91 Clock A	CH90 Clock D	CH89 R/WE1	CH88 R/WE0	CH87 RB_enable2	CH86 RB_enable1	CH85 ASF_counter	CH84 ASF_RAM2	CH83 ASF_RAM1	CH82 Boarsel 2	CH81 Boarsel 1	CH80 Boarsel 0
Read back 2 & 1 disabled, serial load									0	0						
Read back 2 disabled & 1 enabled									0	1						
Read back 2 enabled & 1 disabled									1	0						
Read back 2 & 1 enabled, RC running									1	1						

Init values: channels CH95-CH80

Function	CH95 ISAFUD	CH94 IESYNC	CH93 Reset	CH92 Clock F	CH91 Clock A	CH90 Clock D	CH89 R/WE1	CH88 R/WE0	CH87 RB_enable2	CH86 RB_enable1	CH85 ASF_counter	CH84 ASF_RAM2	CH83 ASF_RAM1	CH82 Boarsel 2	CH81 Boarsel 1	CH80 Boarsel 0
	1	1	1	1	1	0	1	1	0	0	1	1	1	1	1	1
	F				B				3				F			

We pulse generation



40 ns we-pulse is generated, when both R/WEs changes polarity!
That way one I/O-cycle is saved!