Pin allocation of the heating Digital I/O Registers 7/8/08

MPV924 ***register 2, 4 and 6*** *(connectors P6-8) used in the heating DDS control.*

MPV924 Register 1 Heating DDS control

Channel	Signal	Description	Active	MPV	Address + Base
CH_48	DataL_0	Data bit 0	High/Low	out	byte1, Addr +C_7
CH_49	DataL_1	Data bit 1	High/Low	out	
CH_50	DataL_2	Data bit 2	High/Low	out	
CH_51	DataL_3	Data bit 3	High/Low	out	
CH_52	DataL_4	Data bit 4	High/Low	out	
CH_53	DataL_5	Data bit 5	High/Low	out	
CH_54	DataL_6	Data bit 6	High/Low	out	
CH_55	DataL_7	Data bit 7	High/Low	out	
CH_56	DataH_0		High/Low	in	byte_0 Addr + C_6
CH_57	DataH_1		High/Low	in	
CH_58	DataH_2		High/Low	in	
CH_59	DataH_3		High/Low	in	
CH_60	DataH_4		High/Low	in	
CH_61	DataH_5		High/Low	in	
CH_62	DataH_6		High/Low	in	
CH_63	DataH_7		High/Low	in	
CH_64	AD00	Address 00	High/Low	out	byte_1, Addr +C_9
CH_65	AD01	Address 01	High/Low	out	
CH_66	AD02	Address 02	High/Low	out	
CH_67	AD03	Address 03	High/Low	out	
CH_68	AD04	Address 04	High/Low	out	
CH_69	AD05	Address 05	High/Low	out	
CH_70	AD06	Address 06	High/Low	out	
CH_71	AD07	Address 07	High/Low	out	
CH_72	AD08	Address 08	High/Low	out	byte_0, Addr +C_8
CH_73	AD09	Address 09	High/Low	out	
CH_74	AD10	Address 10	High/Low	out	
CH_75	AD11	Address 11	High/Low	out	
CH_76	AD12	Address 12	High/Low	out	
CH_77	AD13	Address 13	High/Low	out	
CH_78	AD14	Address 14	High/Low	out	
CH_79	AD15	Address 15	High/Low	out	
CH_80	BoardSel0	Board select bit 0	High/Low	out	byte1, Addr +C_B
CH_81	BoardSel1	Board select bit 1	High/Low	out	
CH_82	BoardSel2	Board select bit 2	High/Low	out	
CH_83	ASF_RAM1	Amplitude Scale Factor RAM 1 selected	Low	out	
CH_84	ASF_RAM2	Amplitude Scale Factor RAM 2 selected	Low	out	
CH_85	ASF_counter	ASF counters loading selected	Low	out	
CH_86	RB_enable1	Read Back from AD9953_I	Low	out	
CH_87	RB_enable2	Read Back from AD9953_II	Low	out	
CH_88	R/WE0	Read (H) / Write pair 0 (L H)	High/Low	out	byte_0 Addr +C_A
CH_89	R/WE1	Read (H) / Write pair 1 (H L)	High/Low	out	
CH_90	Clock D	Eval. Board clock D	▲	out	
CH_91	Clock A	Eval. Board clock A	▲	out	
CH_92	Clock F	Eval. Board clock F	▲	out	
CH_93	Reset	Board's reset	low	out	
CH_94	IESYNC	Enables sync_FUD to go to the DDSs	low	out	
CH_95	ISAFUD	Synchronization clock for the DDSs	▲	out	
CH_32	SD_out1	Serial data out from DDS1	High/Low	in	byte1, Addr +C_5
CH_33	SD_out2	Serial data out from DDS2	High/Low	in	
CH_34	RUNVALID	DDS-carrier board stopped	Low	in	
CH_35	Spare_5	Spare			
CH_36	Spare_6	Spare			
CH_37	Spare_7	Spare			
CH_38	Spare_8	Spare			
CH_39	Spare_9	Spare			
CH_40	Spare_10	Spare			
CH_41	Spare_11	Spare			
CH_42	Spare_12	Spare			
CH_43	Spare_13	Spare			
CH_44	Spare_14	Spare			
CH_45	Spare_15	Spare			
CH_46	Spare_16	Spare			
CH_47	Spare_17	Spare			