Pin allocation of the FPDP-connector of the DDS Carrier board

FPDP board connector

pin	Signal	pin	signal
80	DataH_7	79	DataH_6
78	DataH_5	77	DataH_4
76	GND	75	DataH_3
74	DataH_2	73	DataH_1
72	DataH_0	71	GND
70	DataL_7	69	DataL_6
68	DataL_5	67	DataL_4
66	GND	65	DataL_3
64	DataL_2	63	DataL_1
62	DataL_0	61	GND
60	AD15	59	AD14
58	AD13	57	AD12
56	GND	55	AD11
54	AD10	53	AD09
52	AD08	51	GND
50	AD07	49	AD06
48	AD05	47	AD04
46	GND	45	AD03
44	AD02	43	AD01
42	AD00	41	GND
40	IESYNC	39	ISAFUD
38	Reset	37	Clock F
36	GND	35	Clock A
34	Clock D	33	R/WE1
32	R/WE0	31	GND
30	RB_enable2	29	RB_enable1
28	ASF_counter	27	ASF_RAM2
26	GND	25	ASF_RAM1
24	BoardSel2	23	BoardSel1
22	BoardSel0	21	GND
20	Spare_17	19	Spare_16
18	Spare_15	17	Spare_14
16	GND	15	Spare_13
14	Spare_12	13	Spare_11
12	Spare_10	11	GND
10	Spare_9	9	Spare_8
8	Spare_7	7	Spare_6
6	GND	5	Spare_5
4	RUNVALID	3	SD_out2
2	SD_out1	1	GND

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MPV924 registers

	I/O-Channel	Signal	Description	Addr
P6	CH_48	DataL_0	Data bit 0 the lower data byte of	Base + C7
	CH_49	DataL_1	Data bit 1 the connector P6 is	
	CH_50	DataL_2	Data bit 2 programmed to be as an	
	CH_51	DataL_3	Data bit 3 output of MPV	
	CH_52	DataL_4	Data bit 4	
	CH_53	DataL_5	Data bit 5	
	CH_54	DataL_6	Data bit 6	
	CH_55	DataL_7	Data bit 7	
	CH_56	DataH_0	Data bit 0 the higher data byte of	Base + C6
	CH_57	DataH_1	Data bit 1 the connector P6 is	
	CH_58	DataH_2	Data bit 2 programmed to be as an	
	CH_59	DataH_3	Data bit 3 input of MPV	
	CH_60	DataH_4	Data bit 4	
	CH_61	DataH_5	Data bit 5	
	CH_62	DataH_6	Data bit 6	
	CH_63	DataH_7	Data bit 7	
P7	CH_64	AD00	Address 00	Base + C9
	CH_65	AD01	Address 01	
	CH_66	AD02	Address 02	
	CH_67	AD03	Address 03	
	CH_68	AD04	Address 04	
	CH_69	AD05	Address 05	
	CH_70	AD06	Address 06	
	CH_71	AD07	Address 07	
	CH_72	AD08	Address 08	Base + C8
	CH_73	AD09	Address 09	
	CH_74	AD10	Address 10	
	CH_75	AD11	Address 11	
	CH_76	AD12	Address 12	
	CH_77	AD13	Address 13	
	CH_78	AD14	Address 14	
	CH_79	AD15	Address 15	
P8	CH_80	BoardSel0	Board select bit 0	Base + CB
	CH_81	BoardSel1	Board select bit 1	
	CH_82	BoardSel2	Board select bit 2	
	CH_83	ASF_RAM1	Amplitude Scale Factor RAM 1 selected	
	CH_84	ASF_RAM2	Amplitude Scale Factor RAM 2 selected	
	CH_85	ASF_counter	ASF counters loading selected	
	CH_86	RB_enable1	Read Back from AD9953_I	
	CH_87	RB_enable2	Read Back from AD9953_II	
	CH_88	R/WE0	Read (H) / Write pair 0 (L H)	Base + CA
	CH_89	R/WE1	Read (H) / Write pair 1 (H L)	
	CH_90	Clock D	Eval. Board clock D	
	CH_91	Clock A	Eval. Board clock A	
	CH_92	Clock F	Eval. Board clock F	
	CH_93	Reset	Board's reset	
	CH_94	IESYNC	Enables sync_FUD to go to the DDSs	
	CH_95	ISAFUD	Synchronization clock for the DDSs	
P5	CH_32	SD_out1	Serial data out from DDS1	Base + C5
	CH_33	SD_out2	Serial data out from DDS2	
	CH_34	RUNVALID	DDS-carrier board stopped	
	CH_35	Spare_5	Spare	
	CH_36	Spare_6	Spare	
	CH_37	Spare_7	Spare	
	CH_38	Spare_8	Spare	
	CH_39	Spare_9	Spare	
	CH_40	Spare_10	Spare	Base + C4
	CH_41	Spare_11	Spare	
	CH_42	Spare_12	Spare	
	CH_43	Spare_13	Spare	
	CH_44	Spare_14	Spare	
	CH_45	Spare_15	Spare	
	CH_46	Spare_16	Spare	
	CH_47	Spare_17	Spare	